Pradyun Narkadamilli

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EDUCATION

University of Illinois Urbana-Champaign, M.S. in Electrical and Computer Engineering   4.0/4.0 GPA, May 2027
Thesis advised by Prof. Nam Sung Kim & Assistant Prof. Dong Kai Wang

University of Illinois Urbana-Champaign, B.S. in Computer Engineering   4.0/4.0 GPA, May 2025
University Honors (Bronze Tablet), Highest Honors, IEEE HKN Honor Society
Bradley J. Griffis Endowed Scholarship, John and Sheila Woythal Scholarship

Relevant Coursework: Advanced Computer Architecture, Advanced VLSI Design, Digital IC Design, Networking, Parallel Computer Architecture, Operating Systems, Advanced Parallel Programming, Vector Space Signal Processing

PUBLICATIONS

Compiler and System Optimizations for the gem5 Simulator   ISPASS 2026
Ha Neul Park, Siddharth Agarwal, **Pradyun Narkadamilli**, Kiung Jung, Yongjun Park, Ipoom Jeong and Nam Sung Kim

RESEARCH

Server RISC-V CPU Architectures (*PIs: Nam Sung Kim, Dong Kai Wang*)   *Ongoing*
- Working under a grant from Samsung Research (SAIT) to develop next-generation RISC-V server cores
- Currently profiling the effects of microarchitectural enhancements on SoTA processors (Control Instruction Fusion)

Software Prefetching for Datacenter Workloads (*PI: Nam Sung Kim*)   *Ongoing*
- Characterizing front-end bottlenecks in datacenter workloads on modern Intel Xeon processors
- Developing an L2 software prefetching scheme using novel x86 code prefetch hint instructions

Kernel Processing Unit (*PI: Nam Sung Kim*)   *Ongoing*
- Investigating a software/hardware co-design solution to offload kernel workloads onto a small, specialized processor

gem5 Simulator Optimizations (*PI: Nam Sung Kim*)   Jan 2026
- Developed a universal Profile-Guided Optimization methodology to optimize gem5 runtime across various workloads
- When coupled with sub-NUMA clustering heuristics, this methodology boosts simulation throughput by up to 20%

WRAITH: A CGRA Architecture with Timeshared RISC-V Execution Support   Dec 2025
- Designed a packet-switched CGRA architecture that leverages idle functional units to emulate RISC-V cores
- Developed/verified an RTL implementation, taped out on TSMC 65nm at 500MHz via an Apple-sponsored shuttle
- Manuscript in preparation, pending chip bringup in Spring 2026

Design of a Graph-Composable Superscalar RISC-V Core (*PI: Dong Kai Wang*)   Dec 2024
- Worked with Assistant Professor Dong Kai Wang to evaluate ArchGen, a graph-based DSE framework
- Created the first composable architecture, a superscalar inorder RISC-V pipeline with support for a wide backend
- Results were compiled as a Bachelor's Thesis and submitted to UIUC's IDEALS journal in Fall 2024

WORK EXPERIENCE

Research Assistant, UIUC   May 2026

CPU Design Intern (Out-of-Order Core Design Team), SiFive   May 2025 – Aug 2025
- Designed and developed RTL for new hardware data prefetcher mechanism targeting L2/L3 cache hierarchy
- Implemented various performance, power, and debug features across Out-of-Order core's Load-Store Unit

ASIC Design Intern (Fabric IP Design Team), Microsoft   May 2024 – Aug 2024
- Developed scheduler subsystem to mitigate power rail droop during mesh packet transmission on Cobalt SoC
- Designed and implemented RTL modules to aggregate and regulate traffic/system events across fabric mesh
- Migrated various release-time packaging deliverables to reusable targets for in-house automation tool

FPGA Design Intern, IMC Trading   Jun 2023 – Aug 2023
- Developed system to filter/publish critical network messages to host from FPGA, reducing PCIe load by 50%
- Designed, implemented, and verified RTL modules to unpack, tag, and arbitrate between multiple UDP streams
- Created testbenches on Verilator-based verification stack, then prototyped C++ API for new networking interface

VLSI Design Teaching Assistant   Jan 2026 – Present
- Developing curriculum and supporting office hours for various VLSI labs (StdCell/Processor layout, PNR, etc.)

Computer Architecture Head Teaching Assistant, UIUC   May 2025 – Dec 2025
Computer Architecture Course Assistant   Feb 2024 – May 2025
- Directed logistics, curriculum, and tooling for UIUC's capstone computer engineering course
- Developed specification, rubric, and documentation for new RISC-V out-of-order processor Senior Design project
- Directly mentored 20+ students through the design, development, and optimization of the out-of-order project
- Ported existing simulation models and tooling to Verilator, yielding over 200x speedup in processor benchmarking

Operating Systems Course Assistant, UIUC   Aug 2023 – Present
- Hosted office hours for class projects (ex: IA-32/RISC-V kernel) and led exam review sessions for 150+ students
- Composed course materials like course notes, exam problems, review materials, etc.

President, ACM SIGArch sigarch.net   Dec 2023 – May 2025
- Curated, created, and presented educational material for UIUC's premier computer architecture club.

Vice President, WaggleNet Research Group wagglenet.org   Nov 2021 – Jan 2023
- Led 7-person team researching computer vision software for embedded motion tracking using OpenCV
- Fully migrated data storage and logging mechanisms to the cloud using AWS Cognito, DynamoDB, and Lambda
- Integrated Raspberry Pi-based dataloggers with aforementioned AWS pipeline to track temp, humidity, etc.

PROJECTS

Superscalar Out-of-Order RISC-V CPU
Created a speculative out-of-order RISC-V CPU with an ERR architecture, implementing the RV32IM spec.
- Supports 1-8 issues/instruction commits per cycle, multiple integer execution units, variable size issue queues, etc.
- Optional parameters to change issue queue scheduling, branch predictor (TAGE), cache timing/associativity, etc.
- Synthesized dual-issue/commit core with L1 caches on FreePDK's 45nm process node at 800MHz, a standing record

NES Emulator pradyun.net/work/naes
Replicated commercial Nintendo Entertainment System (NES) SoC on DE-10 Lite FPGA.
- System can play standard iNES-formatted ROMs on a Motorola 6502 core, video output is displayed over VGA
- Designed logic for PPU (architecture-specific GPU), peripheral emulation hardware, and memory interfaces

GPU Hypergraph Partitioner
Adapted the BiPart hypergraph partitioning algorithm to admit better parallelism in EDA applications on GPUs.
- Implemented the new partitioning algorithm for NVIDIA GPUs in CUDA, using Thrust library for common algorithms
- Gained up to 5x in cut quality improvement and 8x speedup on the Titan EDA benchmark relative to BiPart

Evaluating Subsampling Algorithms for Graph-Signal Interpolation
Conducted a survey of GSP literature to evaluate the interpolation accuracy of modern subsampling methods.
- Reproduced findings of prior studies by Antonio Ortega on modern data models and larger graph signals
- Expanded signal recovery results to encompass Graph Fourier Transform and algorithmic node ranking methods

TECHNICAL SKILLS

General: SystemVerilog, Verilog, Python, C, C++, [ba]sh scripting, Rust, Linux Systems, x86, RISC-V, CUDA, ELisp
Tools: Synopsys VCS, Verdi, Design Compiler, Virtuoso, Innovus, Verilator, Vivado, Quartus, gem5, git