Pradyun Narkadamilli

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Education

University of Illinois Urbana-Champaign, B.S in Computer Engineering — 4.0/4.0 GPA, May 2025

Bradley J. Griffis Endowed Scholarship, John and Sheila Woythal Scholarship
IEEE HKN Honor Society, Dean's List (Fall 2021-Present)

Relevant Coursework: Advanced Computer Architecture, VLSI Design, Digital IC Design, Analog IC Design, Operating Systems, Communication Networks, Parallel Programming, Vector Space Signal Processing

Research

ArchGen: A Graph Framework for Microarchitecture Search and Generation — *In Progress*

- Working with Assistant Professor Dong Kai Wang on ArchGen, a graph-based design space exploration framework
- Created the first composable architecture, a superscalar inorder RISC-V pipeline with support for a wide backend

PANIQ: Perceptron AugmeNted Issue Queues for Out-Of-Order Processor — May 2024

- *Final research paper for ECE 511: Advanced Computer Architecture*
- All evaluations and findings were constructed by using the gem5 architectural simulator

Evaluating Subsampling Algorithms for Graph-Signal Interpolation — May 2024

- *Final research paper for ECE 513: Vector Space Signal Processing*
- Expanded upon the findings of studies by Antonio Ortega, expanded results to algorithmic node ranking methods

Work Experience

CPU Design Intern, SiFive — May 2025

ASIC Design Intern (Fabric IP Design Team), Microsoft — May 2024 – Aug 2024

- Developed scheduler subsystem to mitigate power rail droop during mesh packet transmission on Cobalt SoC
- Designed and implemented RTL modules to aggregate and regulate traffic/system events across fabric mesh
- Implemented more robust error checking and template generation within in-house automation tool
- Migrated various release-time packaging deliverables to reusable targets for in-house automation tool

FPGA Design Intern, IMC Trading — Jun 2023 – Aug 2023

- Developed system to filter/publish critical network messages to host from FPGA, reducing PCIe load by 50%
- Designed and implemented RTL modules to unpack, tag, and arbitrate between multiple UDP streams
- Created testbenches on Verilator-based verification stack, then prototyped C++ API for new networking interface

Computer Architecture Course Assistant, UIUC — Feb 2024 – Present

- Directly mentored 20+ students in the design, development, and optimization of an out-of-order RISC-V core
- Ported existing simulation models and tooling to Verilator, yielding over 200x speedup in processor benchmarking

Operating Systems Course Assistant, UIUC — Aug 2023 – Present

- Hosted office hours for class projects (ex: IA-32/RISC-V kernel) and led exam review sessions for 150+ students
- Composed course materials like course notes, exam problems, review materials, etc.

President, ACM SIGArch sigarch.net — Dec 2023 – Present

- Curated, created, and presented educational material for UIUC's premier computer architecture club.

Projects

Superscalar Out-of-Order RISC-V CPU

Created a speculative out-of-order RISC-V CPU with an ERR architecture, implementing the RV32IM spec.

- Supports 1-8 issues/instruction commits per cycle, multiple integer execution units, variable size issue queues, etc.
- Optional parameters to change issue queue scheduling, branch predictor (TAGE), cache timing/associativity, etc.
- Synthesized dual-issue/commit core with L1 cache on FreePDK's 45nm process node at 800MHz, a standing record

NES Emulator pradyun.net/work/naes

Replicated commercial Nintendo Entertainment System (NES) SoC on DE-10 Lite FPGA.

- System can play standard iNES-formatted ROMs on a Motorola 6502 core, video output is displayed over VGA
- Designed PPU (architecture-specific GPU), peripheral emulation hardware, and memory interfaces
- Demoed at ECE 385 Showcase, running games like Ice Climber, Pac-Man, and Super Mario Bros.

Technical Skills

General: SystemVerilog, Verilog, Python, C, C++, [ba]sh scripting, Rust, Linux Systems, x86, RISC-V, CUDA, ELisp
Tools: Synopsys VCS, Verdi, Design Compiler, Virtuoso, Innovus, Verilator, Vivado, Quartus, gem5, git